

# EE 434

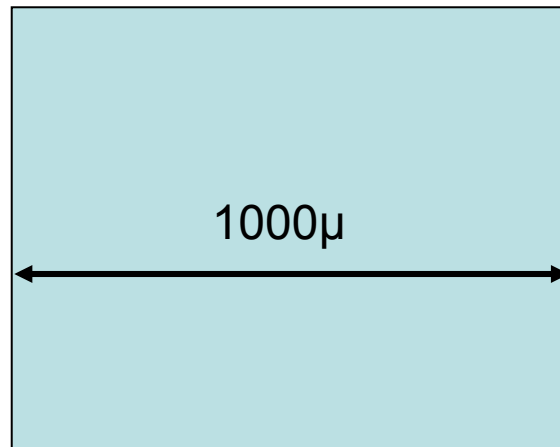
## Lecture 3

### Basic Concepts

Historical Background, Feature Sizes and Yield

## Quiz 1

How many minimum-sized MOS transistors can be placed on a square die that is  $1000\mu$  on a side in a 65nm process? (Neglect any bonding pads needed to get the signals to the outside world. Assume factor of 10 overhead for spacing between transistors).



And the number is ....

1

8

3

5

4

6

9

7

2

And the number is ....

1

7

3

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8

6

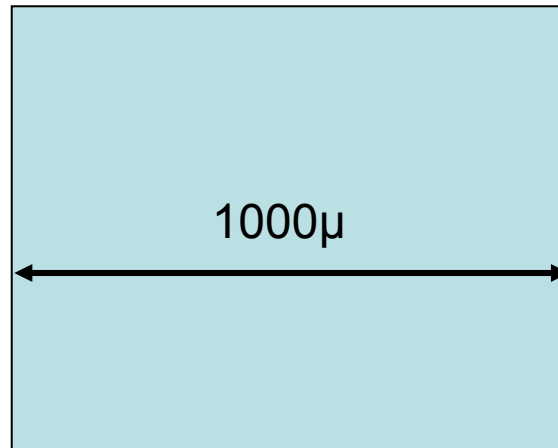
9

2

5

## Quiz 1

How many minimum-sized MOS transistors can be placed on a square die that is  $1000\mu$  on a side in a  $65\text{nm}$  process? (Neglect any bonding pads needed to get the signals to the outside world. Assume factor of 10 overhead for spacing between transistors.)



Solution:

$$n_{\text{Tran}} \cong \frac{1}{10} \frac{A_{\text{die}}}{A_{\text{tran}}}$$

$$n_{\text{Tran}} \cong \frac{1}{10} \frac{(1000\mu)^2}{(65\text{nm})^2} = \mathbf{23.6 \text{ million}}$$

## Review from Last Time

- Sophisticated Integrated CAD Toolsets are extensively used in the industry to design integrated circuits
  - Minimize the chances of an error
  - Real asset to (and not a competitor of) the engineer
  - Critical to pay attention to what tools tell you
- Feature size good metric for characterizing capabilities of a process
  - State of the art at about 65nm
  - Pitch sometimes used instead of feature size
  - Drawn and actual features may differ
  - Bragging rights focus on actual rather than drawn features
- Yield often determined by statistically independent events

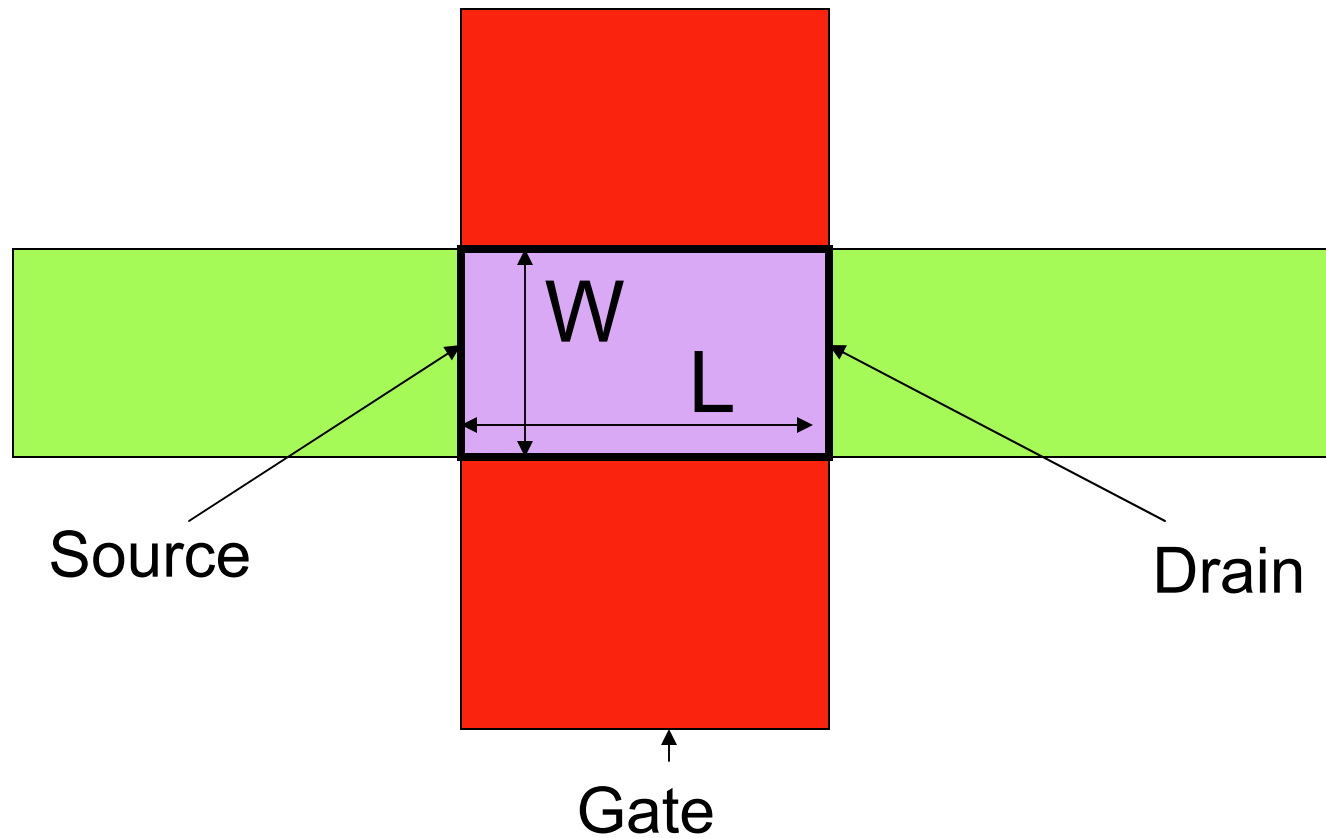
$$Y = P^n$$

- Cost of Wafers in \$800 to \$3000 range depending on size and process

$$C_{\text{per unit area}} \cong \$2.5 / \text{cm}^2$$

Review from Last Time

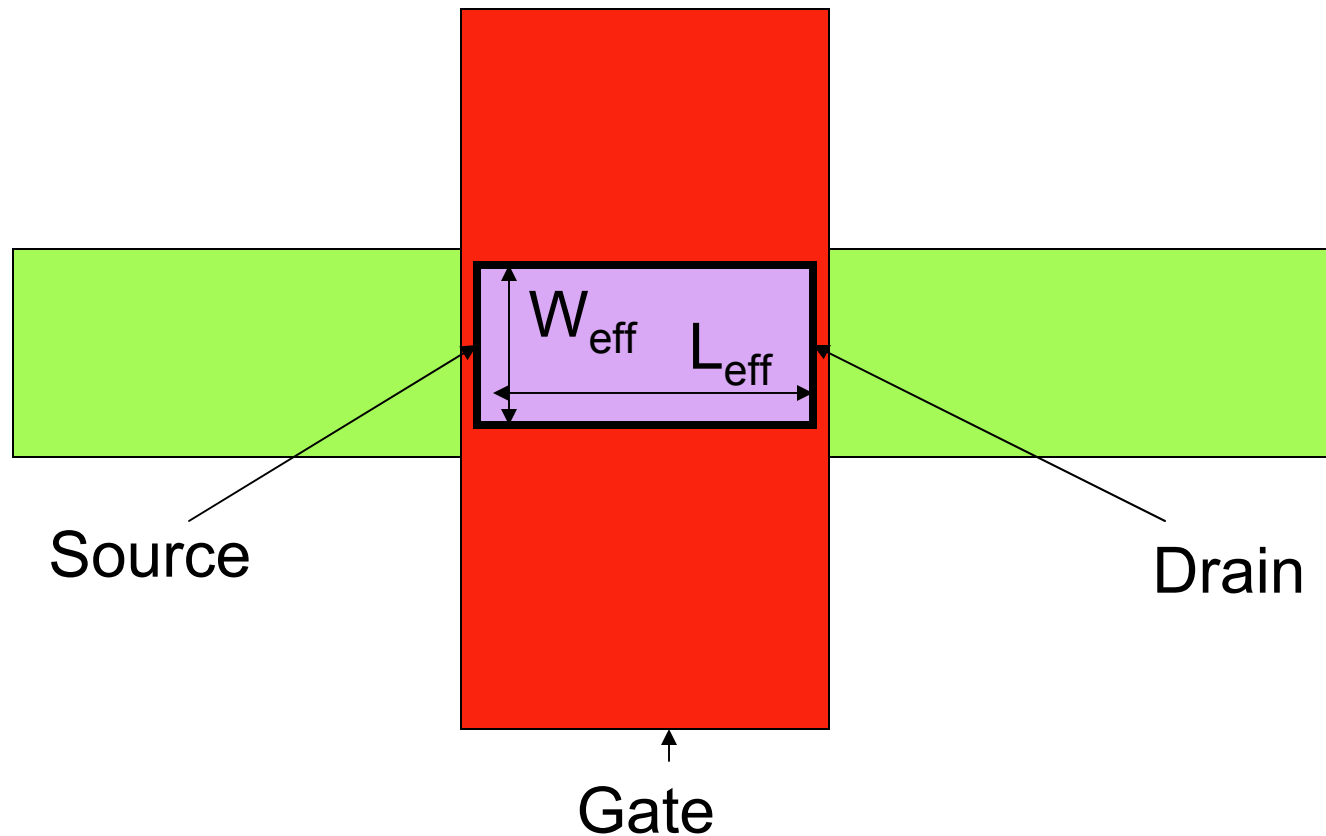
# MOS Transistor



Actual Drain and Source at Edges of Channel

Review from Last Time

# MOS Transistor



Effective Width and Length Generally  
Smaller than Drawn Width and Length

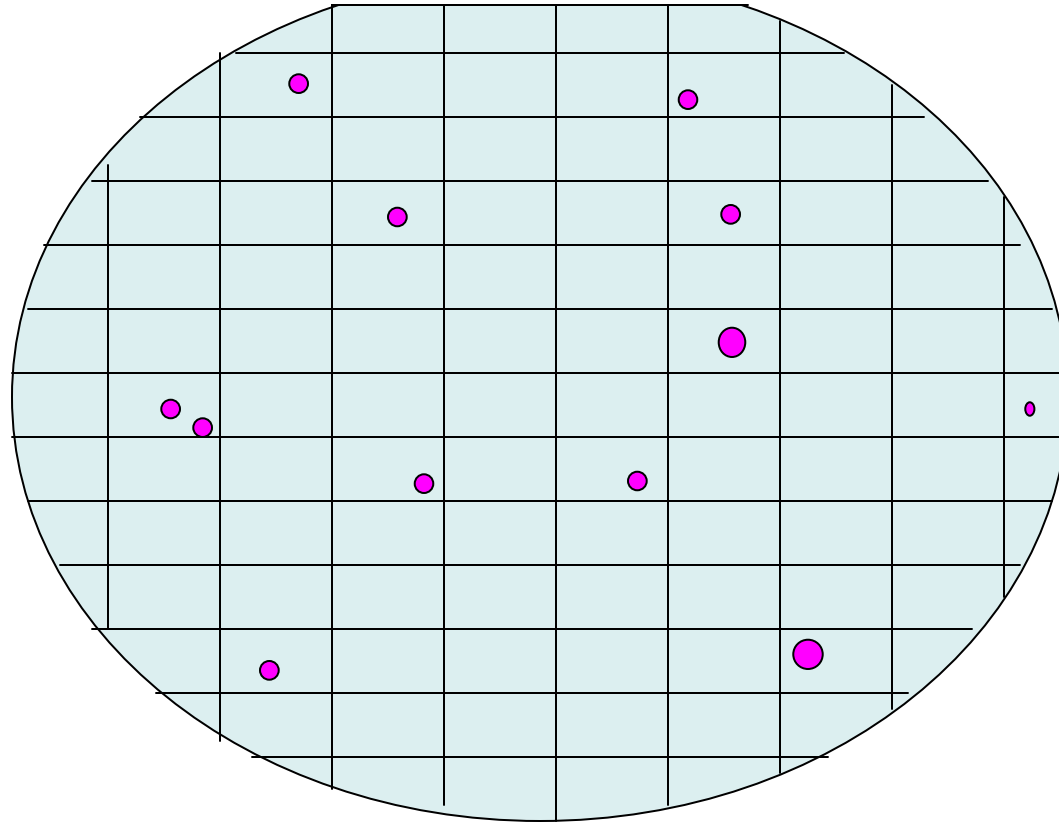



# Size of Atoms and Molecules in Semiconductor Processes

Silicon:	Average Atom Spacing	$2.7 \text{ \AA}$
	Lattice Constant	$5.4 \text{ \AA}$
$\text{SiO}_2$	Average Atom Spacing	$3.5 \text{ \AA}$
	Breakdown Voltage	$5 \text{ to } 10 \text{ MV/cm} = 5 \text{ to } 10 \text{ mV/\AA}$
Air		$20 \text{ KV/cm}$

Physical size of atoms and molecules place fundamental limit on conventional scaling approaches

# Defects in a Wafer



 Defect

- Dust particles and other undesirable processes cause defects
- Defects in manufacturing cause yield loss

# Yield Issues and Models

- Defects in processing cause yield loss
- The probability of a defect causing a circuit failure increases with die area
- The circuit failures associated with these defects are termed **Hard Faults**
- This is the major factor limiting the size of die in integrated circuits
- Wafer scale integration has been a “gleam in the eye” of designers for 3 decades but the defect problem continues to limit the viability of such approaches
- Several different models have been proposed to model the hard faults

# Yield Issues and Models

- Parametric variations in a process can also cause circuit failure or cause circuits to not meet desired performance specifications (this is of particular concern in analog and mixed-signal circuits)
- The circuits failures associated with these parametric variations are termed **Soft Faults**
- Increases in area, judicious layout and routing, and clever circuit design techniques can reduce the effects of soft faults

# Hard Fault Model

$$Y_H = e^{-Ad}$$

$Y_H$  is the probability that the die does not have a hard fault

$A$  is the die area

$d$  is the defect density (typically  $1\text{cm}^{-2} < d < 2\text{cm}^{-2}$ )

Industry often closely guards the value of  $d$  for their process

Other models, which may be better, have the same general functional form

# Soft Fault Model

Soft fault models often dependent upon design and application

Often the standard deviation of a parameter is dependent upon the reciprocal of the square root of the parameter sensitive area

$$\sigma = \frac{\rho}{\sqrt{A_k}}$$

$\rho$  is a constant dependent upon the architecture and the process

$A_k$  is the area of the parameter sensitive area

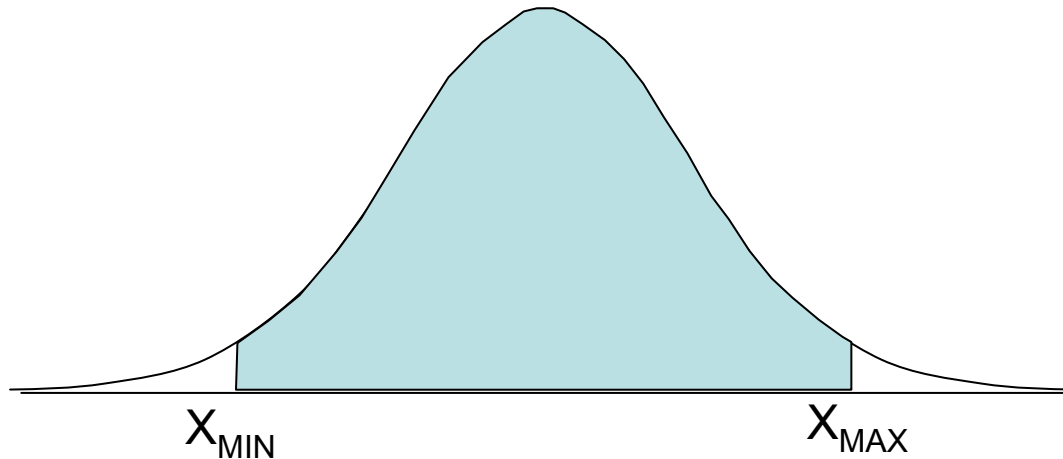
# Soft Fault Model

$$P_{\text{SOFT}} = \int_{X_{\text{MIN}}}^{X_{\text{MAX}}} f(x) dx$$

$P_{\text{SOFT}}$  is the soft fault yield

$f(x)$  is the probability density function of the parameter of interest

$X_{\text{MIN}}$  and  $X_{\text{MAX}}$  define the acceptable range of the parameter of interest



Some circuits may have several parameters that must meet performance requirements

# Soft Fault Model

If there are  $k$  parameters that must meet parametric performance requirements and if the random variables characterizing these parameters are uncorrelated, then the soft yield is given by

$$Y_S = \prod_{j=1}^k P_{\text{SOFT}_j}$$



# Overall Yield

If both hard and soft faults affect the yield of a circuit, the overall yield is given by the expression

$$Y = Y_H Y_S$$

# Cost Per Good Die

The manufacturing costs per good die is given by

$$C_{\text{Good}} = \frac{C_{\text{FabDie}}}{Y}$$

where  $C_{\text{FabDie}}$  is the manufacturing costs of a fab die and  $Y$  is the yield

There are other costs that must ultimately be included such as testing costs, engineering costs, etc.

Example: Assume a die has no soft fault vulnerability, a die area of  $1\text{cm}^2$  and a process has a defect density of  $1.5\text{cm}^{-2}$

- a) Determine the hard yield
- b) Determine the manufacturing cost per good die if 8" wafers are used and if the cost of the wafers is \$1200

# Solution

$$\text{a) } Y_H = e^{-Ad}$$

$$Y = e^{-1\text{cm}^2 \cdot 1.5\text{cm}^{-2}} = 0.22$$

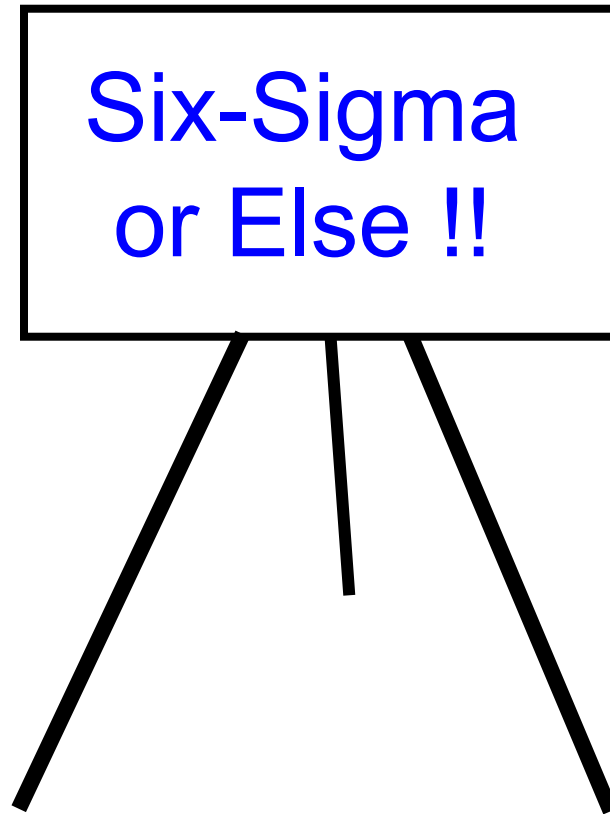
$$\text{b) } C_{\text{Good}} = \frac{C_{\text{FabDie}}}{Y}$$

$$C_{\text{FabDie}} = \frac{C_{\text{Wafer}}}{A_{\text{Wafer}}} A_{\text{Die}}$$

$$C_{\text{FabDie}} = \frac{\$1200}{\pi(4\text{in})^2} 1\text{cm}^2 = \$3.82$$

$$C_{\text{Good}} = \frac{\$3.82}{0.22} = \$17.37$$

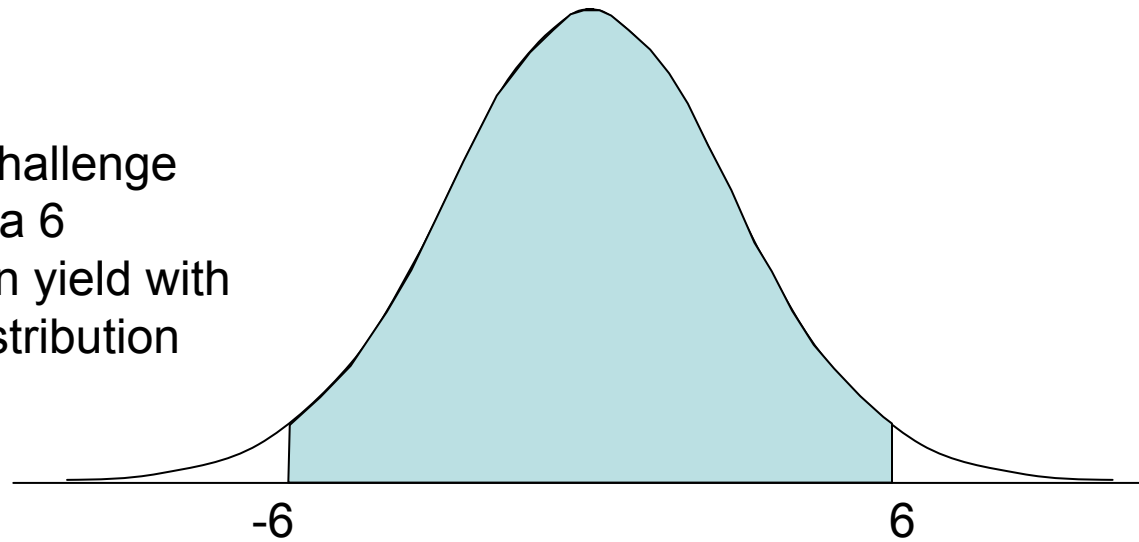
# Meeting the Real Six-Sigma Challenge



Example: Determine the maximum die area if the circuit yield is to meet the “six sigma” challenge (Assume a defect density of  $1\text{cm}^{-2}$  and only hard yield loss). Is it realistic to set six-sigma die yield expectations on the design and process engineers?

Solution:

The “six-sigma” challenge requires meeting a 6 standard deviation yield with a Normal (0,1) distribution



$$Y_{6\text{sigma}} = 2F_N(6) - 1$$

Solution cont:

<b>No Sigma</b>	<b>Yield</b>	<b>Defect Rate</b>
1	0.682689492	0.317311
2	0.954499736	0.0455
3	0.997300204	0.0027
4	0.999936658	6.33E-05
5	0.999999427	5.73E-07
6	0.9999999980	1.97E-09
7	0.9999999999974	2.56E-12

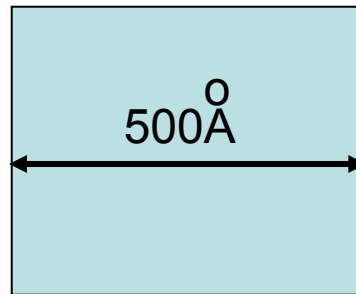
Six-sigma performance is approximately 2 defects in a billion !

Solution cont:

$$Y_H = e^{-Ad}$$

$$A = \frac{-\ln(Y_H)}{d}$$

$$A = \frac{-\ln(.99999999980)}{1\text{cm}^{-2}} = 2.0\text{E}-9\text{cm}^2 = 2.5\text{E}5(\text{\AA})^2$$



This is orders of magnitude less than the area needed to fabricate even a single transistor



Solution cont:

Is it realistic to set six-sigma die yield expectations on the design and process engineers?

The best technologies in the world have orders of magnitude too many defects to build any useful integrated circuits with die yields that meet six-sigma performance requirements !!

Is it realistic to set six-sigma feature yield expectations on individual features in a process?

# How reliable must a feature be?

Consider a circuit with  $n=5E9$  features (this is not a particularly large number of features in a current process.) and a target yield of 90%.

$$P = e^{\frac{\log_e Y}{n}} = e^{\frac{\log_e 0.9}{5E3}} = 0.999999999979$$

$P$  is the probability that this feature must be good to achieve the 90% yield.

The corresponding defect probability is

$$1 - 0.999999999979 = 2.1E-11$$

This corresponds to an average of about .02 defects in a billion !

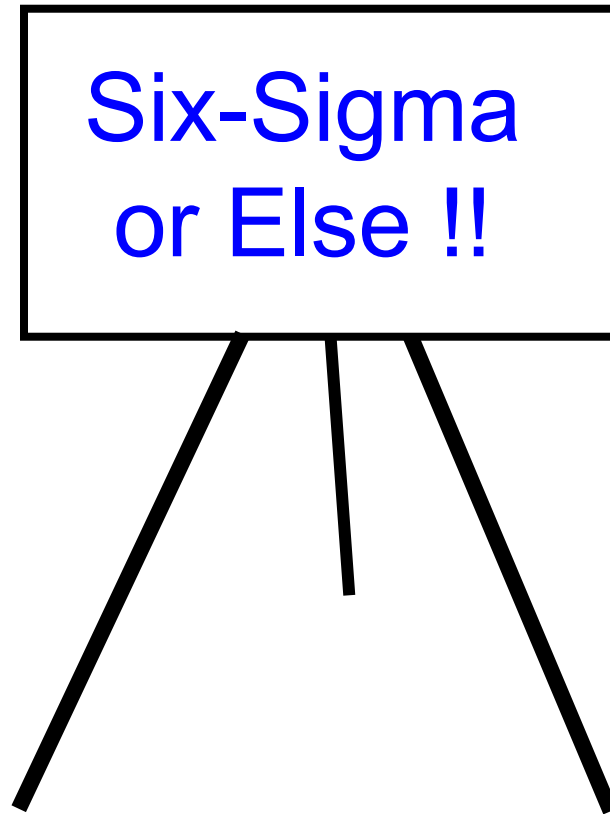
Six-sigma performance requires to meeting 2 defects in a billion performance so this is dramatically more stringent than the 6 sigma level !

## Is it realistic to set six-sigma feature yield expectations on individual features in a process?

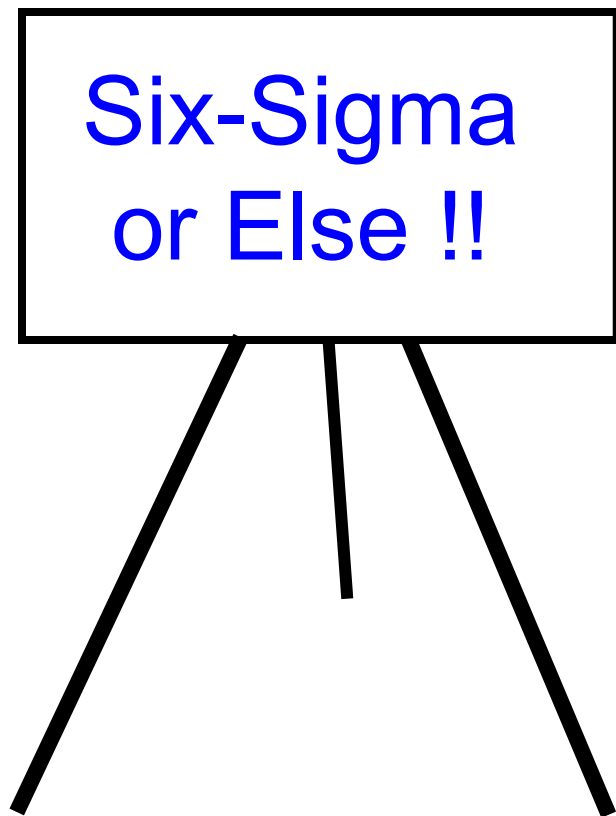
Six-sigma feature yield is too low to expect acceptable die yield !

- Six-sigma yield expectations can be way too stringent or way too lax depending upon what step is being considered in the manufacturing process !!
- Arbitrarily establishing six-sigma expectations on all steps in a process will guarantee financial disaster !!
- Yield expectations should be established based upon solid mathematical formulations relating the overall manufacturing costs to the market potential of a product

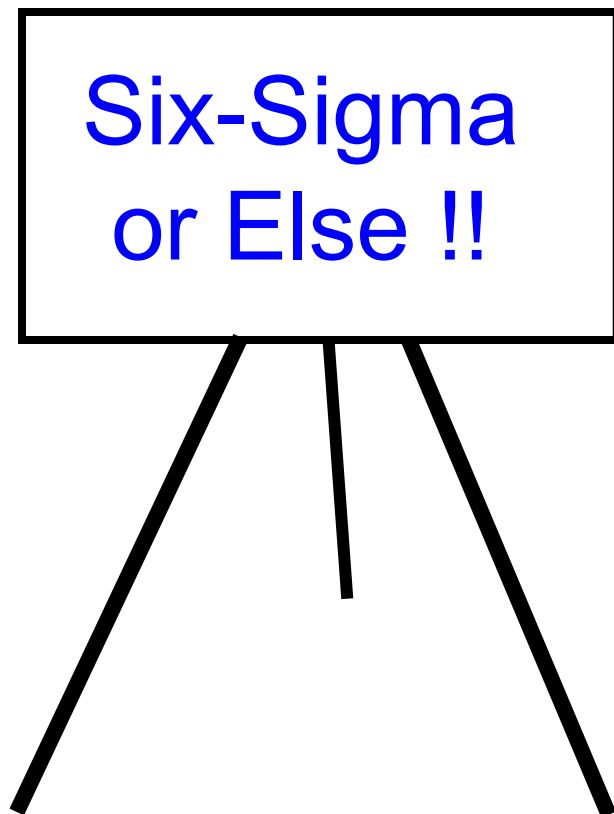
# Meeting the Real Six-Sigma Challenge



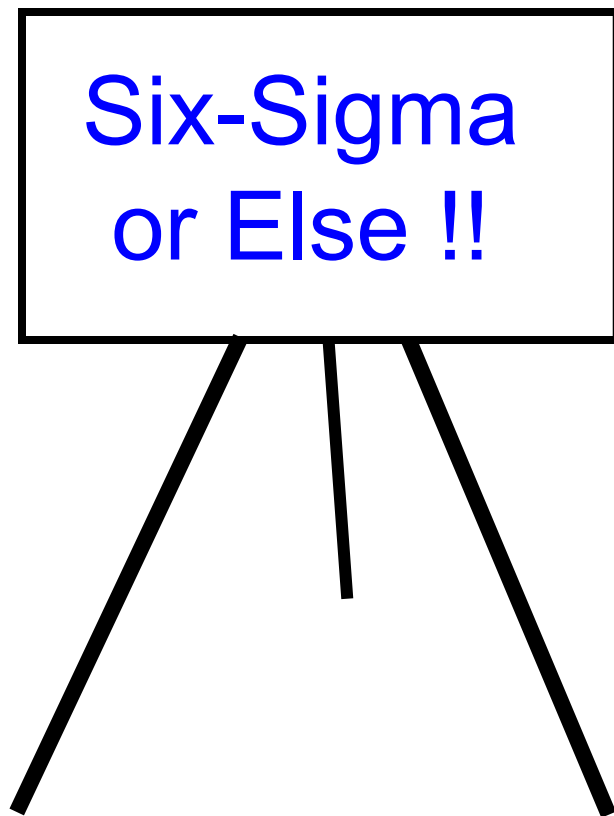
# Meeting the real Six-Sigma Challenge



# Meeting the real Six-Sigma Challenge



# Meeting the real Six-Sigma Challenge





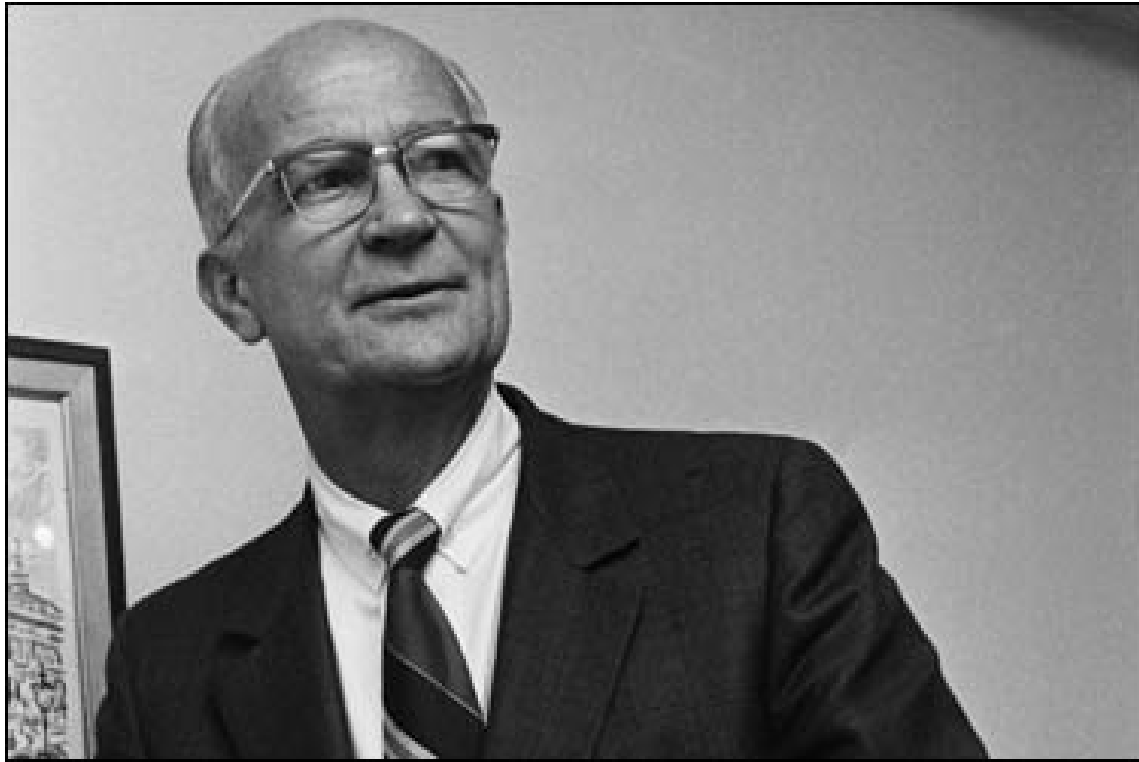
# Key Historical Developments

- 1925,1935 Concept of MOS Transistor Proposed (Lilienfield and Heil)
- 1947 BJT Conceived and Experimentally Verified (Bardeen, Bratin and Shockley of Bell Labs)
- 1959 Jack Kilby (TI) and Bob Noyce (Fairchild) invent IC
- 1963 Wanless (Fairchild) Experimentally verifies MOS Gate

# Naming the Transistor

From the group at Bell Labs

“We have called it the transistor, T-R-A-N-S-I-S-T-O-R, because it is resistor or semiconductor device which can amplify electrical signals as they are transferred through it from input to output terminals. It is, if you will, the electrical equivalent of a vacuum tube amplifier. But there the similarity ceases. It has no vacuum, no filament, no glass tube. It is composed entirely of cold, solid substances.”



William Shockley

<http://www.time.com/time/time100/scientist/profile/shockley03.html>

## William Shockley

He fathered the transistor and brought the silicon to Silicon Valley but is remembered by many only for his noxious racial views

By GORDON MOORE

The transistor was born just before Christmas 1947 when John Bardeen and Walter Brattain, two scientists working for William Shockley at Bell Telephone Laboratories in Murray Hill, N.J., observed that when electrical signals were applied to contacts on a crystal of germanium, the output power was larger than the input. Shockley was not present at that first observation. And though he fathered the discovery in the same way Einstein fathered the atom bomb, by advancing the idea and pointing the way, he felt left out of the momentous occasion.

Shockley, a very competitive and sometimes infuriating man, was determined to make his imprint on the discovery. He searched for an explanation of the effect from what was then known of the quantum physics of semiconductors. In a remarkable series of insights made over a few short weeks, he greatly extended the understanding of semiconductor materials and developed the underlying theory of another, much more robust amplifying device — a kind of sandwich made of a crystal with varying impurities added, which came to be known as the junction transistor. By 1951 Shockley's co-workers made his semiconductor sandwich and demonstrated that it behaved much as his theory had predicted.

Not content with his lot at Bell Labs, Shockley set out to capitalize on his invention. In doing so, he played a key role in the industrial development of the region at the base of the San Francisco Peninsula. It was Shockley who brought the silicon to Silicon Valley.

In February 1956, with financing from Beckman Instruments Inc., he founded Shockley Semiconductor Laboratory with the goal of developing and producing a silicon transistor. He chose to establish this start-up near Palo Alto, where he had grown up and where his mother still lived. He set up operations in a storefront — little more than a Quonset hut — and hired a group of young scientists (I was one of them) to develop the necessary technology. By the spring of 1956 he had a small staff in place and was beginning to undertake research and development.

This new company, financed by Fairchild Camera & Instrument Corp., became the mother organization for several dozen new companies in Silicon Valley. Nearly all the scores of companies that are or have been active in semiconductor technology can trace the technical lineage of their founders back through Fairchild to the Shockley Semiconductor Laboratory. Unintentionally, Shockley contributed to one of the most spectacular and successful industry expansions in history.

*Editor's note:*

In 1963 Shockley left the electronics industry and accepted an appointment at Stanford. There he became interested in the origins of human intelligence. Although he had no formal training in genetics or psychology, he began to formulate a theory of what he called dysgenics. Using data from the U.S. Army's crude pre-induction IQ tests, he concluded that African Americans were inherently less intelligent than Caucasians — an analysis that stirred wide controversy among laymen and experts in the field alike.

[54] **SEMICONDUCTOR DEVICE**  
 [72] Inventor: Jack St. Clair Kilby, Dallas, Tex.  
 [73] Assignee: Texas Instruments Incorporated, Dallas, Tex.  
 [22] Filed: Jan. 29, 1962  
 [21] Appl. No.: 169,557

**Related U.S. Application Data**

[63] Continuation-in-part of Ser. No. 791,602, Feb. 6, 1959, Pat. No. 3,138,743, and a continuation-in-part of 811,476, May 6, 1959, abandoned, and a continuation-in-part of 811,486, May 6, 1959, Pat. No. 3,138,744.

[52] U.S. Cl. .... 317/235, 317/234, 317/101  
 [51] Int. Cl. .... H01I 19/00  
 [58] Field of Search ..... 317/234, 235, 101, 231

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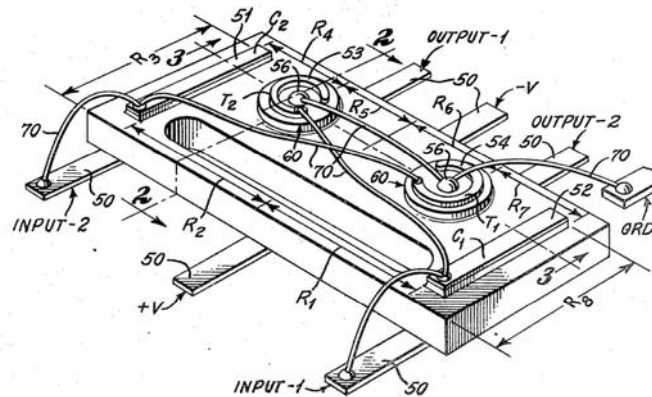
Primary Examiner—James D. Kallam  
 Attorney—James O. Dixon, Andrew M. Hassell, Robert C.

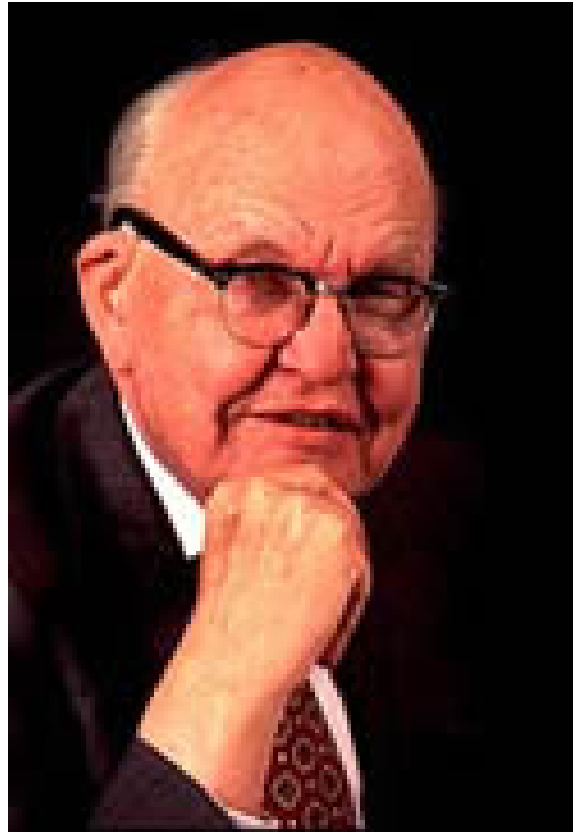
Peterson and Stevens, Davis, Miller and Mosher

**EXEMPLARY CLAIM**

1. A semiconductor device comprising:
  - a. a wafer of semiconductor material having two major faces;
  - b. said wafer being so shaped as to define a plurality of regions within said wafer and adjacent to one of said major faces;
  - c. at least some of said regions being electrically isolated within said wafer from others of said regions;
  - d. said regions having at least one portion thereof extending to said one major face;
  - e. at least some of said portions having selected locations on said one major face for electrical contact to said region;
  - f. an insulating material on said one major face of the wafer excluding at least said selected locations;
  - g. at least one electrically conductive area in contact with said insulating material and spaced from said wafer thereby;
  - h. said electrically conductive area being disposed in cooperative relationship with respect to a selected one of said isolated regions so as to provide the electrical function of a discrete electrical circuit component; and
  - i. a plurality of metallic interconnections providing electrically conductive paths between said selected locations on different ones of said regions and between another selected one of said locations and said electrically conductive area.

4 Claims, 33 Drawing Figures





Jack Kilby

<http://www.ti.com/corp/docs/kilbyctr/jackstclair.shtml>

There are few men whose insights and professional accomplishments have changed the world. Jack Kilby is one of these men. His invention of the monolithic integrated circuit - the microchip - some 45 years ago at Texas Instruments (TI) laid the conceptual and technical foundation for the entire field of modern microelectronics. It was this breakthrough that made possible the sophisticated high-speed computers and large-capacity semiconductor memories of today's information age.

Mr. Kilby grew up in Great Bend, Kansas. With B.S. and M.S. degrees in electrical engineering from the Universities of Illinois and Wisconsin respectively, he began his career in 1947 with the Centralab Division of Globe Union Inc. in Milwaukee, developing ceramic-base, silk-screen circuits for consumer electronic products.

In 1958, he joined TI in Dallas. During the summer of that year working with borrowed and improvised equipment, he conceived and built the first electronic circuit in which all of the components, both active and passive, were fabricated in a single piece of semiconductor material half the size of a paper clip. The successful laboratory demonstration of that first simple microchip on September 12, 1958, made history.

Jack Kilby went on to pioneer military, industrial, and commercial applications of microchip technology. He headed teams that built both the first military system and the first computer incorporating integrated circuits. He later co-invented both the hand-held calculator and the thermal printer that was used in portable data terminals.



April 25, 1961

R. N. NOYCE

2,981,877

SEMICONDUCTOR DEVICE-AND-LEAD STRUCTURE

Filed July 30, 1959

3 Sheets-Sheet 1

FIG-1

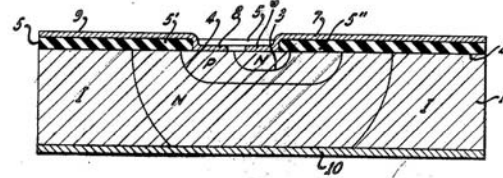
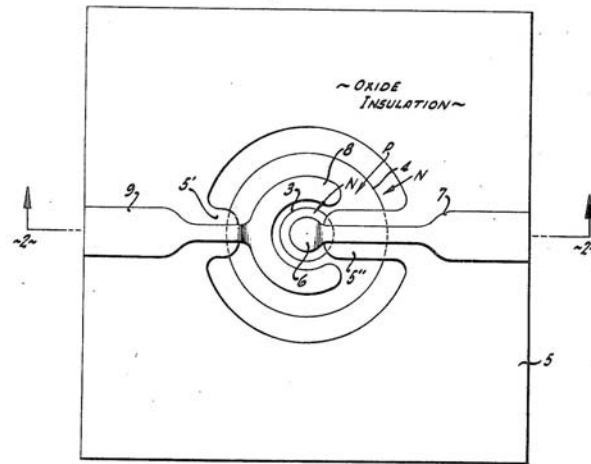


FIG-2

INVENTOR.  
ROBERT N. NOYCE  
BY *Leppinott & Ralls*  
ATTORNEYS



Robert Noyce

<http://www.idealfinder.com/history/inventors/noyce.htm>

Robert Norton Noyce was born December 12, 1927 in Burlington, Iowa. A noted visionary and natural leader, Robert Noyce helped to create a new industry when he developed the technology that would eventually become the microchip. Noted as one of the original computer entrepreneurs, he founded two companies that would largely shape today's computer industry—Fairchild Semiconductor and Intel.

Bob Noyce's nickname was the "Mayor of Silicon Valley." He was one of the very first scientists to work in the area -- long before the stretch of California had earned the Silicon name -- and he ran two of the companies that had the greatest impact on the silicon industry: Fairchild Semiconductor and Intel. He also invented the integrated chip, one of the stepping stones along the way to the microprocessors in today's computers.

Noyce, the son of a preacher, grew up in Grinnell, Iowa. He was a physics major at Grinnell College, and exhibited while there an almost baffling amount of confidence. He was always the leader of the crowd. This could turn against him occasionally -- the local farmers didn't approve of him and weren't likely to forgive quickly when he did something like steal a pig for a college luau. The prank nearly got Noyce expelled, even though the only reason the farmer knew about it was because Noyce had confessed and offered to pay for it.

While in college, Noyce's physics professor Grant Gale got hold of two of the very first transistors ever to come out of Bell Labs. Gale showed them off to his class and Noyce was hooked. The field was young, though, so when Noyce went to MIT in 1948 for his Ph.D., he found he knew more about transistors than many of his professors.

After a brief stint making transistors for the electronics firm Philco, Noyce decided he wanted to work at Shockley Semiconductor. In a single day, he flew with his wife and two kids to California, bought a house, and went to visit Shockley to ask for a job -- in that order.

As it was, Shockley and Noyce's scientific vision -- and egos -- clashed. When seven of the young researchers at Shockley semiconductor got together to consider leaving the company, they realized they needed a leader. All seven thought Noyce, aged 29 but full of confidence, was the natural choice. So Noyce became the eighth in the group that left Shockley in 1957 and founded Fairchild Semiconductor.

Noyce was the general manager of the company and while there invented the integrated chip -- a chip of silicon with many transistors all etched into it at once. Fairchild Semiconductor filed a patent for a semiconductor integrated circuit based on the planar process on July 30, 1959. That was the first time he revolutionized the semiconductor industry. He stayed with Fairchild until 1968, when he left with Gordon Moore to found Intel.

At Intel he oversaw Ted Hoff's invention of the microprocessor -- that was his second revolution.

At both companies, Noyce introduced a very casual working atmosphere, the kind of atmosphere that has become a cultural stereotype of how California companies work. But along with that open atmosphere came responsibility. Noyce learned from Shockley's mistakes and he gave his young, bright employees phenomenal room to accomplish what they wished, in many ways defining the Silicon Valley working style was his third revolution.

# Key Historical Developments

- 1971 Intel Introduces 4004 microprocessor (2300 transistors, 10u process)



# Silicon Gate MOS 4004

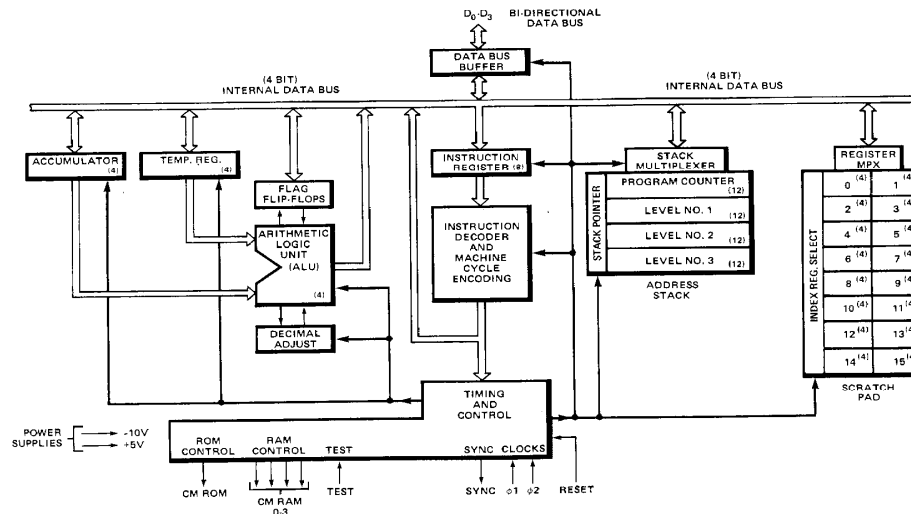
## SINGLE CHIP 4-BIT P-CANNEL MICROPROCESSOR

- 10.8 Microsecond Instruction Cycle
- CPU Directly Compatible With MCS-4 ROMs and RAMs
- Easy Expansion—One CPU can Directly Drive up to 32,768 Bits of ROM and up to 5120 Bits of RAM
- 4-Bit Parallel CPU With 46 Instructions
- Instruction Set Includes Conditional Branching, Jump to Subroutine and Indirect Fetching
- Binary and Decimal Arithmetic Modes

The Intel<sup>®</sup>4004 is a complete 4-bit parallel central processing unit (CPU). It is designed to be used in test systems, terminals, billing machines, process control and random logic replacement applications. The 4004 easily interfaces with keyboards, switches, displays, A-D converters, printers and other peripheral equipment.

The CPU can directly address 4K 8-bit instruction words of program memory and 5120 bits of data storage RAM. Sixteen index registers are provided for temporary data storage. Up to 16 4-bit input ports and 16 4-bit output ports may also be directly addressed.

The 4004 is fabricated with P-channel silicon gate MOS technology.



MICRO-COMPUTERS

End of Lecture 3